sensor to image

SVDK Smart Vision Development Kit

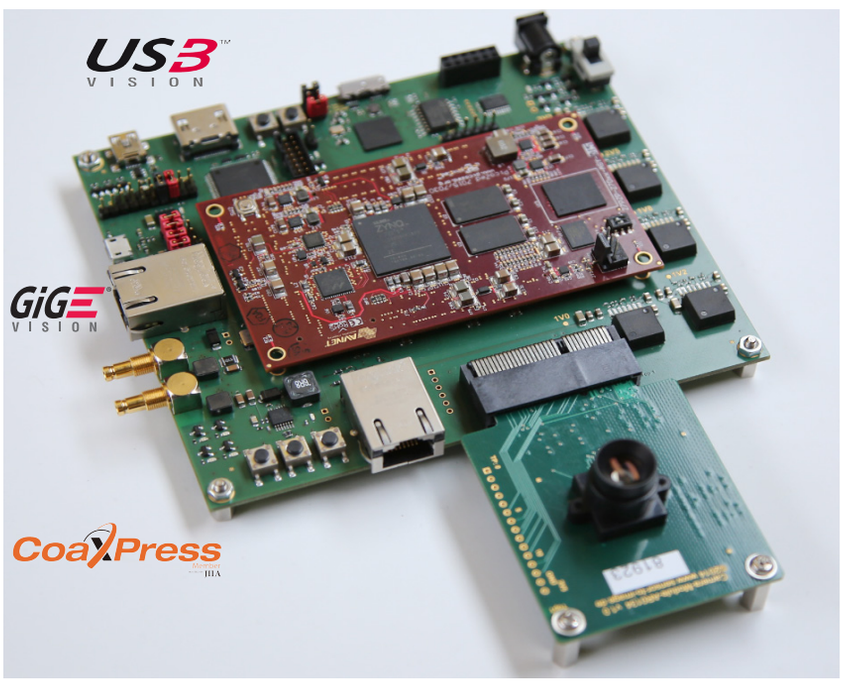
CoaXPress®, USB Vision® and GigE Vision® – compliant test platform

All interfaces on one baseboard with XILINX ZYNQ FPGA

FPGA on AVNET PicoZED module

With SVDK we have, for the first time, all major industrial vision interfaced on one platform to test:

- **ZYNQ interface to CCD/CMOS vision sensors**
- **GigE Vision compliant camera design, PL or PS based**
- **USB3 Vision compliant camera design**
- **CXP compliant camera design**
- **GigE Vision compliant HOST design, PL or PS based**
- **CXP compliant HOST design**
- **all IP reference designs out of the box and verified by AIA and JIIA standard organisations**
- **PC software support for GEV and U3V with GenAPI compliant Windows and LINUX application**
- **Genicam compliant XML for all interfaces**



SVDK Evaluation Board

CXP - FPGA Core

CoaXPress, CXP, is a rugged interface with a bandwidth of up to 25GBit (4 links) and cable length up to 200m. The standard is GenICam based and defined and tested by JIIA. On this hardware a single lane CXP6 DEVICE (camera) and HOST (frame grabber) design is supported, which allows net video data rate of 5GBit. The DEVICE and HOST reference designs are fully CXP compliant and certified by JIIA.

U3V - FPGA Core

USB3 Vision, U3V, is based on the 5GBit technology of standard USB3 components and allows maybe the most cost efficient high speed camera design today. Nevertheless U3V itself and of course the U3V SVDK implementation is fully compliant to Genicam and U3V, and certified by AIA to allow an easy start with Plug-and-Play camera interfaces at cable lengths of 3m at net video speed of 4GBit.

GEV - FPGA Core

GigE Vision, GEV, is based on field proven Ethernet cables and jacks. It is using UDP with reliability extensions, can run at speeds from 10MBit to 10GBit and supports cables length of up to 100m. The IP core for a GEV DEVICE and HOST is fully compliant to AIA GEV specification and testing. It is implemented on the SVDK with a speed of 1GBit and can run at net video data rate of 950MBit on PL design and 300MBit with the PS variant.

All IP on SVDK comes with the kit in a 30min time bombed variant with downloadable VIVADO based design. All designs include a step-by-step tutorial and are ready to go within a few minutes. The IP around the kit can be extended to production versions on other XILINX FPGA families.

FPGA RESOURCES

MODULE	CXP-HOST	CXP-DEVICE	USB3 VISION	GIGE VISION
FPGA based streaming protocol implementation				
– Slice registers	3542	3549	3134	3229
– Slice lookup tables	4058	4151	3161	3651
– Block RAMs	11	6	7	4
– Maximum clock frequency	155 MHz	221 MHz	177 MHz	201 MHz
Framebuffer				
– Slice registers	–	–	2198	2198
– Slice lookup tables	–	–	1877	1877
– Block RAMs	–	–	2	2
– Maximum clock frequency	–	–	233 MHz	233 MHz
MicroBlaze based control protocol implementation				
– Slice registers	2797	4750	–	4240
– Slice lookup tables	2959	4264	–	3864
– BlockRAMs	14	16	–	8
– Minimum clock frequency	62.5 MHz	62.5 MHz	–	62.5 MHz
MAC				
– eMACs	–	–	–	–
– Slice registers	–	–	–	584
– Slice lookup tables	–	–	–	652
– BlockRAMs	–	–	–	–
– Maximum clock frequency	–	–	–	125 MHz

values are post synthesize only and based on platform specific reference designs, other architectures might have different resource usage

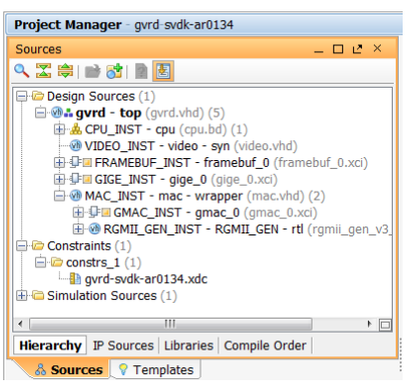
OPERATING SYSTEMS

MODULE	WIN 7/8	UBUNTU 12.04	CENTOS 6
Sphinx Library (.dll/.a)	•	•	•
Sphinx Filter Driver / U3V Driver	•	•	•
Sphinx GEV / U3V Viewer	•	•	•

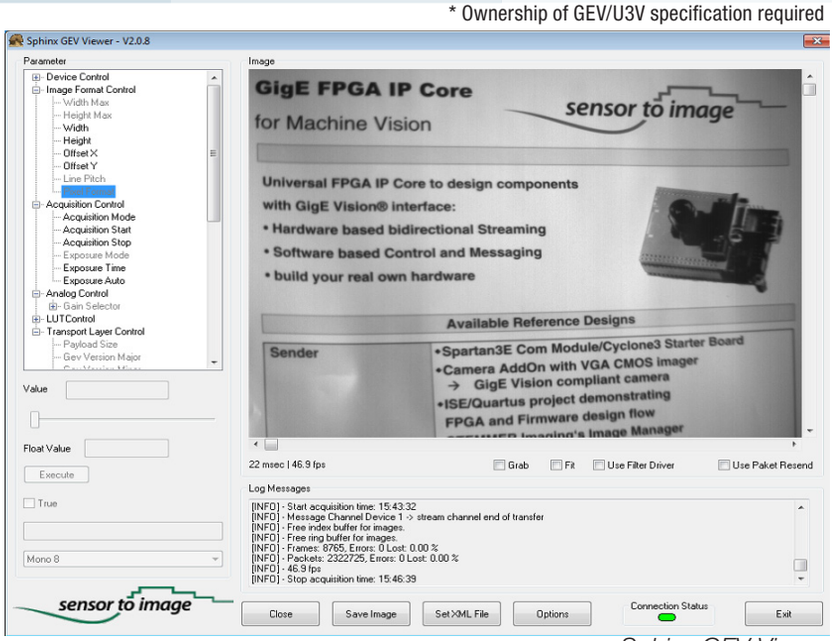
SOURCE CODE

MODULE	STANDARD EDITION	COMMUNITY EDITION
Sphinx Library (.dll/.a)		•*
Sphinx Filter Driver / U3V Driver		•*
Sphinx GEV / U3V Viewer	•	•

* Ownership of GEV/U3V specification required



Vivado Project Hierarchy



Sphinx GEV Viewer

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